REMARKS

Claim 1 has been amended to emphasize that sample/latch circuit inputs are connected "exclusively" to the coding unit, as illustrated in Fig. 3. In addition, claim 1 has been grammatically revised to emphasize that the originally claimed "plurality of control signal lines" are between the sample/latch circuits and the D/A converters, as also illustrated in Fig. 3 as well as in Fig. 4.

Reconsideration of the present patent application is respectfully requested in view of the following remarks.

I. Response to Rejections Under 35 U.S.C. § 102

The rejection of claims 1, 4 and 7 under 35 U.S.C. § 102 (e) as being anticipated by the US Laid Open No. 2003/0085859 (Lee et al.).is respectfully traversed on the grounds that, in the circuit of Lee:

- The inputs to register 100 of Lee are not exclusively connected to the source of the gamma curve data D_{V1R}~D_{V9R} *etc.* (which corresponds to the coding unit), but rather are connected both to the gamma data source and to a timing signal "GMA_load"—in contrast, the claimed sample/latch circuits need no external timer but rather transmit received data in real time directly to the D/A converters; and
- The alleged sample/latch circuits 100 of Lee are not each connected by a plurality of signal lines to the D/A converters 200—Only a single signal lines connects the respective D/A converters VGMA(+), VGMA(-), *etc.* of Lee to the memory 100, whereas the claimed sample/latch circuits are

connected by signal lines 231 and 232 as illustrated in Fig. 4 of the present application.

The first distinction has to do with the different nature of the claimed sample/latch circuits and the memory 100 of Lee. This is not merely a matter of obvious design choice, but rather a fundamental difference with significant consequences concerning operation of the respective circuits. In particular, Lee register 100 stores data according to a timing signal "GMA_load" supplied by an external timing circuit and illustrated in Fig. 2 of Lee, whereas the claimed sample-latch circuits simply transmit data received from the coding unit in real time to the D/A converters, without an external timing input *and without conventional data storage*. Accordingly, those skilled in the art will understand that the claimed reference voltage generator is independent of the driving circuit and different from the data drivers of the Lee patent. It might be possible to argue that a sample/latch circuit is a type of "data storage" and therefore analogous in a sense to the register 100 of Lee, but it is a data storage that merely coordinates pass through of data from the coding unit to the D/A converters and not a timed data storage of the type disclosed by Lee. This distinction has now been more positively recited, by reciting that the sample/latch circuit inputs are connected exclusively to the coding unit, and therefore this feature of the claimed invention cannot reasonably be said to be taught by Lee.

The second distinction was already recited in the previous amendment, and has to do with the fact that, as illustrated in Fig. 2 of the Lee patent, only a single line connects the respective D/A converters of block 200 with the cells of register 100. Again, this is a matter of differences in timing, with Lee relying on data storage and

external timing and the claimed invention using a two- data line connection that permits coded data to be transmitted on one line and timing signal for the conversion to be transmitted on a second line. Lee clearly only includes single lines between the register and respective D/A converters, and therefore does not disclose or suggest the use of "a *plurality* of signal lines," as claimed.

As a result of these distinctions, the claimed invention eliminates the need for costly memory and complicated timing arrangements. Because of the use of exclusively-connected sample/latch circuits and a plurality of signal lines, the coding unit of the driving circuit generates a plurality of coded data according to a plurality of characteristic curves at the same time, and the three "separate and regulable" Gamma reference voltages are generated in real time. As a result, during the generation of these three Gamma reference voltages, no storing process is executed, and no "storage device", such as a register" for storing the encoded data, is required. In contrast, as described in paragraph [0026], line 13 to paragraph [0027], line 5 of the specification of the Lee patent, the gamma register 100 receives the digital gamma data through a plurality of data buses from a timing controller (not shown) and stores the digital gamma data in response to the gamma load signal GMA_load, as shown in FIG. 2 of the Lee patent. That is, the gamma register 100 stores the digital gamma data. Therefore, the gamma register 100 does not sample/latch the encoded data (gamma data) during the generation of the reference voltages (gamma reference voltages).

Based on the above, it will be appreciated that the coding unit of the present application is not a "time controller", since the coding unit of the present application

generates a plurality of encoded data according to a plurality of characteristic curves (Gamma curves respectively for three primary colors R, G, B). In fact, the coding unit and the reference voltage generator are independent from the ordinary driving circuit, such as the timing controller and the related circuits of the driving circuit of an LCD device.

As a result, in view of the foregoing amendment to claim 1, the driving circuit of claim 1 of the present patent application is different from the driving circuit of the cited Lee patent, and withdrawal of the rejection of claim 1 based on the Lee patent is respectfully requested. The other claims are directly or indirectly dependent on claim 1, and thus are distinguished from the prior art by the same reason.

II. Response to Rejections Under 35 U.S.C. § 103

Examiner indicates that claim 9 of the present patent application is rejected under 35 U.S.C. § 103(a) as being unpatentable over US Laid Open No. 2003/0085859 (Lee et al.).

As described above, the applicant has amended claim 1 of the present application, for reciting that the driving circuit for solving the color dispersion as claimed in claim 1 of the present application does not include a "storage device" and no storing process is executed during the generation of the reference voltages.

Therefore, as the dependent claim of the amended claim 1, the driving circuit as claimed in claim 9 of the present application cannot be anticipated by the Lee et al, even though the usage of the buffers is well known in the art.

CONCLUSION

In view of the foregoing remarks, reconsideration and allowance of the application are now believed to be in order, and such action is hereby solicited. If any points remain in issue that the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

BACON & THOMAS, PLLC

By: BENJAMIN E. URCIA
Registration No. 33,805

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BACON & THOMAS, PLLC
625 Slaters Lane, 4th Floor
Alexandria, Virginia 22314

Telephone: (703) 683-0500